METHOD AND APPARATUS FOR LOW COST SIGNATURE TESTING FOR ANALOG AND RF CIRCUITS

This application is a continuation-in-part of the inventors' prior application Serial No. 09/575,488, filed May 19, 2000, entitled Method for Testing Circuits, and claims the benefit of the provisional application Serial No. 60/197,749, filed April 18, 2000, entitled ATPG for Prediction of Analog Specifications, and Serial No. 60/203,602, filed May 12, 2000, entitled Test Generation for High Frequency and RF Circuits, each incorporated by reference in their entireties herein.

Background of the Invention

The present invention relates to a method and apparatus for low cost signature testing for testing analog and RF circuits. More particularly, the invention relates to such a method and apparatus for use in manufacturing testing, and for use in monitoring the manufacturing process.

Analog and RF circuits are characterized by a set of performance parameters that typically vary continuously over a range. These performance parameters result from design as modified by variations in the manufacturing process that occur over time. Because of this variation, it is often necessary to test at least some of the circuits produced by a given manufacturing process to ensure that the performance parameters of the circuits fall within given specification limits.

However, traditional testing methods impose an increasing burden in the form of test time as a result of the ever increasing complexity and speeds of analog and RF circuits. For example, straightforward testing employs automated or automatic test equipment ("ATE") to stimulate the circuit under test (CUT) in a manner designed to induce the circuit to provide an output which directly reflects the value of each performance parameter which it is desired to test. The output is used to determine whether the parameter is within specification limits, in which case the CUT is considered "good" or is considered to "pass," or whether the parameter is outside the specification limits, wherein the CUT is considered "bad" or is considered to "fail."

Each performance parameter requires, in general, a specific stimulus appropriate for testing that parameter and a corresponding output measurement, and it is therefore time consuming to step through all of the required test stimuli to obtain the performance parameters of interest in this manner.

Various techniques have been proposed to minimize this test time and, therefore, the cost of testing. Such techniques have attempted to arrive at a single test stimulus effective for discerning whether the CUT passes or fails. For example, S.J. Tsai, "Test vector generation for linear analog devices," International Test Conference, pp. 592-597, 1991, characterizes the circuit as either "good" or "bad" as a result of its response to a stimulus that maximizes the difference in response between circuits having these characterizations. The stimulus is obtained by optimization methods, wherein the impulse responses for good and bad circuits are used as input to an optimization model, the result of which produces the test stimulus.

Alternatively, as in W. Lindermeir, H.E. Graeb and K.J. Antreich, "Design of Robust Test Criteria in Analog Testing," International Conference on Computer Aided Design, pp. 604-611, 1995, a user provides a set of proposed test stimuli, and the method provides for choosing the one that is most effective at discriminating between "good" and "bad" circuits.

Some serious drawbacks of these methods are that neither is applicable to non-linear circuits, and neither provides quantitative information about the circuit performance parameters themselves. Further the method of the latter reference places a demand on the user to provide a set of test stimuli, hence the method provides no assistance in generating or optimizing the test stimuli.

Moreover, an additional problem encountered in testing RF circuits is the need for very high frequencies in the test signal. This imposes an additional cost on testing, as the ATE needed to produce high frequency test signals of arbitrary shape is more complex and difficult to use. Neither of the aforementioned prior art test methodologies has addressed this problem.

Accordingly, there is a need for a method and apparatus for low cost signature testing of both RF and analog circuits that provides more information about circuit performance parameters and provides more information about the manufacturing process.

Summary of the Invention

The method and apparatus for low cost signature testing for analog and RF circuits according to the present invention solves the aforementioned problems and meets the aforementioned needs by providing a model adapted to predict one or more performance parameters characterizing a first electronic circuit produced by a manufacturing process subject to process variation from the output of one or more second electronic circuits produced by the same process in response to a selected test stimulus, and iteratively varying the test stimulus to minimize the error between the predicted performance parameters and corresponding measured values for the performance parameters, for determining an optimized test stimulus.

The optimized test stimulus is applied to manufactured circuits under test for testing the quality of the circuits, and output signatures are obtained. The output signatures thereby obtained are preferably applied to a non-linear model to obtain more accurately predicted performance parameters for the manufactured circuits.

Therefore, it is a principal object of the present invention to provide a novel and improved method and apparatus for low cost signature testing for analog and RF circuits.

It is another object of the invention to provide such a novel and improved method and apparatus for low cost signature testing for analog and RF circuits that efficiently reduces test time and therefore cost.

It is yet another object of the invention to provide such a novel and improved method and apparatus that provides for maximizing prediction accuracy.

It is still another object of the present invention to provide such a method and apparatus for low cost signature testing for analog and RF circuits that provides more information about circuit performance parameters than would otherwise be available.

It is a further object of the present invention to provide such a method and apparatus for low cost signature testing for analog and RF circuits that provides for calibrating for short or long term variations in the manufacturing process.

The foregoing and other objects, features and advantages of the present invention will be more readily understood upon consideration of the following

detailed description of the invention, taken in conjunction with the following drawings.

Brief Description of the Drawings

Figure 1 is a flow chart of a preferred method for developing an optimized test signal as part of a method for low cost signature testing of electronic circuits according to the present invention.

Figure 2 is a preferred form of a test stimulus according to the present invention.

Figure 3 is a flow chart illustrating construction of a non-linear model according to the present invention.

Figure 4 is a flow chart of a preferred method for manufacturing testing according to the present invention using the optimized test stimulus of Figure 1.

Figure 5 is a flow chart for an autocalibration method according to the present invention.

Figure 6 is a flow chart of a preferred method for low cost signature testing of RF electric circuits according to the present invention.

Detailed Description of a Preferred Embodiment

The present application incorporates herein by reference in its entirety the publication by inventors R. Voorakaranam and A. Chatterjee entitled "Test Generation for Accurate Prediction of Analog Specifications," IEEE VLSI Test Symposium, pp. 137-142, 2000. This publication provides mathematical explanation, background and support for methods according to the invention that are described herein in a simplified manner. Also incorporated herein is the inventor's paper, submitted to the International Test Conference 2001, entitled "Low-Cost Signature Testing of RF Circuits," attached hereto as Appendix A.

With reference to Figure 1, a flow chart of a preferred method for low cost signature testing 100 of electronic circuits is shown. Each of the circuits has a set of performance parameters "P(I), I = 1 . . . L, that must fall within a range bounded by a corresponding set of performance specifications. If one or more of the parameters falls outside of the corresponding specification for the parameter, the circuit fails the

test; otherwise, the circuit passes. However, it is an outstanding feature of the present invention that the method and apparatus provide an estimate of the performance parameters as well as indicating whether or not the performance parameters meets their specifications without directly testing them.

The typical context for the method 100 is that there are a number of the electronic circuits "C" obtained from a common manufacturing process for the circuits. The manufacturing process may be characterized by process parameters "Proc(g)", g = 1 . . . G, that will vary about mean values of the process parameters over time. The process parameters form a G-dimensional "process parameter space."

In a step 101, the process parameters Proc(g) are perturbed, one at a time, by a small amount, so that, preferably, there is one perturbed value "Pert(g)" for each process parameter. Correspondingly, in a step 102 of the preferred method 100, one circuit "C(g)" is produced under the process conditions represented by each perturbed value Pert(g).

Turning to step 103, traditional ATE testing is conducted on the circuits "C(g)", i.e., C(1), C(2), . . . C(G), and the circuits' performance parameters "$P_g(i)$", i.e., $P_1(i)$, $P_2(i)$, . . . $P_G(I)$, are obtained in Step 106. For example, one of the performance parameters $P_g(i=1)$ may be the slew rate for the circuit C(g), and another performance parameter $P_g(i=2)$ may be the gain of the circuit C(g) at a particular frequency. The performance parameters of the circuits measured or otherwise obtained in the traditional manner are referred to herein as "actual" performance parameters $P_g(i)_A$. In step 107, "g" is iterated in steps 101 - 106.

In another step 108 of the preferred method, which may be conducted at any time relative to steps 102 to 106, a test stimulus Stim(k) (k = 0, 1, . . . k) is selected. Initially, where k = 0, the test stimulus is selected arbitrarily in anticipation of later, iterative optimization. Preferably, for simplifying the methodology, the test stimulus is selected to be a piece-wise linear function of time having a relatively small number of breakpoints, such as five to ten breakpoints BP (see Figure 2).

The stimulus Stim(k) is physically applied to the circuit C(1) (Step 110), and the circuit's response is measured over time (Step 112). Preferably, the circuit's response to the stimulus is sampled at predetermined regular time intervals Δt to

provide a set of samples forming a "signature" Sig(g,k,t) for the circuit C(g) corresponding to the stimulus Stim(k) at a predetermined time sample t.

In step 113, "g" is iterated in steps 110 and 112, i.e., these steps are carried out with respect to circuits C(2), C(3), . . . C(G). Accordingly, by the conclusion of step 113 for the initial stimulus Stim(k=0), each of the circuits C(g) has been stimulated with the stimulus Stim(0), corresponding signatures Sig(g,0,t) have been determined, and corresponding actual performance parameters $P_1(i)_A$, $P_2(i)_A$, . . . $P_G(Ii_A$ have been measured.

In steps 114a and 114b, the measured signatures and performance parameters for all of the circuits C(g), i.e., $\sum_g$ Sig(g,k,t), and $\sum_g P_g(i)_A$, are provided to a step 115 wherein a linear predictive model LPM(k) is constructed for the present stimulus Stim(k). The linear predictive model is used for predicting performance parameters, wherein "predict" as used herein is synonymous with "estimate" and is not intended to signify foretelling of future events.

The linear predictive model relates the measured signatures $\sum_g$ Sig(g,k,t) to the measured performance parameters $\sum_g P_g(i)_A$, by a set of simultaneous, linear equations. For example, for the stimulus Stim(0), the linear model LPM(0) is a matrix of coefficients representing the solution of simultaneous linear equations relating the measured signatures Sig(g,0,t) to the measured performance parameters $P_g(i)_A$.

Turning to steps 116 - 118, the LPM(k) is used to receive as an input the signatures Sig(g,k,t) and to produce as an output a prediction or estimate of the performance parameters of the circuit $P_g(i,k)_P$, assuming that the signatures Sig(g,k,t) result from stimulating the circuit C(g) with the stimulus Stim(k). In step 120, the predicted performance parameters are compared with the actual performance parameters obtained from step 114b and an error "e(k)" is obtained (Step 122) that is representative of the prediction error for the set of circuits C(g).

It may be noted that there would be no prediction error in predicting the measured performance parameters $P_g(i,k)_A$ for the circuits C(g) from the signatures actually used to obtain the measured performance parameters if the model perfectly mapped measured signatures to measured performance parameters. However, the linear model assumes linear relationships between the performance parameters and the

signatures where these relationships are generally non-linear. Notwithstanding, the error introduced by using a linear model is minimized according to the invention by use of a less costly procedure than would be required for constructing a more accurate, non-linear model.

In practice, each performance parameter will have associated therewith a component of the prediction error, and a total error to be minimized may be defined as the mean squared error summed equally over all of the performance parameters, or the performance parameters may be weighted if desired to emphasize the relative importance of selected parameters. The error may further be defined in other ways as desired without departing from the principles of the invention.

The inventors have recognized that the prediction error "e(k)" depends on the test signal and can be minimized by determining a test signal that is optimum for this purpose. Moreover, by optimizing the test signal to minimize this error, the test signal is made robust in terms of the capability to induce circuits under test, whose performance parameters are subject to further process variations, to produce signatures from which those performance parameters can be predicted.

According to the invention, the prediction error "e(k)" is minimized by iteratively varying the test stimulus Stim(k). Any standard iterative optimization method may be employed for this purpose. The test stimulus Stim(k) is varied by choosing new breakpoints or adding or deleting segments, and repeating steps 103 - 118 (Step 126) until the error "e(k)" falls within an acceptable maximum ζ. This provides an optimized test stimulus $\text{Stim(k)}_{\text{optimized}}$ and a linear predictive model $\text{LPM(k)}_{\text{optimized}}$ that may be used with the optimized test stimulus for use in manufacturing test as discussed below in connection with Figure 3.

Because the linear predictive models LPM(k) consider only small linearized variations in the process parameters, the error "e(k)" is due to linearization errors introduced by the linear model (σ^2 (mdl)) and measurement noise variance (σ^2 (nse)) . A preferred objective or cost function for minimizing the total error "e(k)" = σ^2 (tot) = σ^2 (mdl) + σ^2 (nse)) is:

$$F = \sum k_j, \text{ (for } j = 1 \ldots . n), \text{ where:}$$

$$k_j = 1 + [(1-(\sigma\,(tot)/\zeta]/n \qquad \text{for } \sigma\,(tot) < \zeta, \text{ or}$$

$$k_j = \sigma\,(tot)/\zeta \qquad \text{for } \sigma\,(tot) \geq \zeta,$$

where "n" is the number of circuits sampled. The objective function is preferably minimized as a result of using a genetic algorithm for optimizing the piece-wise linear test stimulus.

As is apparent from Figure 1, revised linear predictive models are preferably constructed for each iteration of the test stimulus. The number of predictive models that are constructed in this iterative process suggests the advantage of using linear models as opposed to non-linear models to optimize the test stimulus. The present inventors have recognized that the test signal optimized using iterative linear models is adequate for testing purposes and the method is significantly less costly than obtaining a non-linear model having greater predictive accuracy, especially where the non-linear model employs an iteratively optimized test stimulus.

All of the aforementioned steps are taken in advance of actual manufacturing testing, where an investment in time may be made without impacting the manufacturing process. For actual manufacturing test, a non-linear predictive model "NLPM" is preferably constructed for use with the optimized test signal $Stim(k)_{optimized}$ found by use of the iteratively determined linear predictive models of steps. A preferred method for constructing the NLPM is provided by J.H. Friedman, "Multivariate Adaptive Regression Splines," *The Annals of Statistics*, Vol. 19, No. 1 1-141, incorporated by reference herein in its entirety. However, other known mathematical methods may be employed for constructing the NLPM as desired without departing from the principles of the invention. Referring to Figure 3, similar to the LPM, the NLPM is constructed to relate measured signature outputs Sig(g,t) from several manufactured "training" circuits ("trng C_g"), as opposed to simulation models. The training circuits are stimulated with $Stim(k)_{optimized}$, and measured performance parameters $P_g(i)_A$ for the training circuits are obtained.

Turning to Figure 4 wherein a manufacturing test process 400 is illustrated, once the optimized test stimulus and NLPM are found and determined, they may be employed in a manufacturing test strategy by applying the optimized test stimulus

$Stim(k)_{optimized}$ to any number of manufactured circuits under test ("mfd. CUT") (Step 402), sampling the outputs of the circuits to obtain signatures therefor (Step 404), applying the signatures to the NLPM (Step 406), and obtaining predicted performance parameters for each of the circuits (Step 408) at the output of the NLPM. In this way, a significant time saving is realized for each test, since a single test stimulus produces an accurate prediction of performance parameters for the circuits.

The manufacturing process used to produce the electronic circuits will shift or drift over time as well as fluctuate differently (either more or less) than at the time of carrying out the construction of the non-linear model NLPM. In other words, the NLPM may not characterize the process adequately as the process changes over time. To detect and correct for this circumstance, a method 500 shown in Figure 5 according to the present invention is preferably used to "autocalibrate" the NLPM. In a preferred form of the method, the signature responses for each manufactured circuit under test (step 502) are obtained from step 404 (Figure 4) and statistically analyzed (step 504). For example, the mean, maximum and minimum value of the signatures for the manufactured devices may be noted. These statistical parameters may be compared to the same kind of parametric data recorded for the training circuits to determine a deviation (step 506). This may be done for each manufactured circuit individually or, preferably, the information obtained from a number of the manufactured circuits may be pooled, the number being chosen to provide a statistically significant inference that the deviation reflects a significant process change. Such a circuit or set of circuits provides one or more "outlier circuits."

Where the deviation in one or more of the parameters for such outlier circuits is determined to have reached a predetermined threshold level (step 508), the NLPM is preferably updated to reflect the additional information provided by the outlier circuits. More particularly, the signature outputs of the outlier circuits are obtained and performance parameters for the outlier circuits are measured (Step 509). An "updated" NLPM is constructed (Step 510) using the outlier circuits as additional data points. More particularly, where the original or previous NLPM is constructed based on a set of training circuits g = G1, the updated NLPM may be similarly constructed based on the set of training circuits g = G1 + the number of outlier circuits, where the outlier circuits are reflective of the changed process. Alternatively, an entirely new

NLPM could be constructed by obtaining additional "new" or "updated" training circuits.

Turning to Figure 6, a method 600 that is particularly adapted for testing RF circuits according to the invention is illustrated. In the method 600, step 110 of the method 100 (see Figure 1) is modified by modulating an RF carrier 20 with the stimulus Stim(k). The modulated RF carrier is applied to the circuit C(g), and its response is measured over time as in step 112. Additional steps 612 and 614 are provided wherein the response is demodulated by the RF carrier and low-pass filtered. A device interface board DIB is provided for modulating the carrier with the test stimuli, demodulating the signature outputs of the circuits under test, and passing the demodulated outputs through a low pass filter LPF.

The modulation/demodulation scheme employed in the method 600 is arbitrary, it being understood that any modulation/demodulation scheme may be employed without departing from the principles of the invention.

Steps according to the present invention that apply an input to one of the models, or obtain an output of the models, may be accomplished in a computer at the instruction of a computer program, which may be embodied in any machine-readable form, such as encoded in volatile or non-volatile semiconductor memory or floppy disk. The models themselves are preferably computerized models, meaning for purposes herein that the models are accessible for use by a computer. Where actual electrical stimuli are applied to actual circuits, or where actual outputs from the actual circuits are obtained, any testing equipment or device known in the art for carrying out these actions may be employed.

It is to be recognized that, while a particular low cost signature test for RF and analog circuits has been shown and described as preferred, other configurations and methods could be utilized, in addition to those already mentioned, without departing from the principles of the invention.

The terms and expressions which have been employed in the foregoing specification are used therein as terms of description and not of limitation, and there is no intention of the use of such terms and expressions of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims which follow.